AMENDMENTS TO THE CLAIMS

1 (currently amended). A compound semiconductor FET comprising:

an AlN layer provided on a substrate;

~~an n-type delta doped III-N layer provided on the AlN layer;~~

~~a plurality of III-N layers provided on the n-type delta doped III-N layer;~~

a plurality of III-N layers provided on the AlN layer;

an n-type delta doped III-N layer interposed between the AlN layer and the plurality of III-N layers, and having dopant concentration for reducing discontinuity of an electric field at an interface between the AlN layer and the III-N layers;

a source electrode;

a gate electrode; and

a drain electrode.

2 (Original). The compound semiconductor FET according to claim 1, wherein the n-type delta doped III-N layer is an n-type delta doped GaN layer,

wherein the plurality of III-N layers comprise a GaN layer and an AlGaN layer formed on the GaN layer, and

wherein the source electrode, the gate electrode, and the drain electrode are provided on the AlGaN layer.

3 (Currently amended). The compound semiconductor FET according to claim 1, further comprising an insulating layer ~~on the AlGaN layer~~ on an uppermost layer of the plurality of III-N layers, wherein the n-type delta doped III-N layer is an n-type delta doped GaN layer,

wherein the plurality of III-N layers comprise a GaN layer and an AlGaN layer formed on the GaN layer,

wherein the source electrode and the drain electrode are provided on the AlGaN layer, and

wherein the gate electrode is provided on the insulating layer.

4 (canceled)

5 (Currently amended). The compound semiconductor FET according to Claim 1, wherein material of the substrate is sapphire,

wherein each of the semiconductor layers ~~is formed of a semiconductor having~~ formed upon the substrate is of a C-plane Ga-surface type, and

wherein sheet doping concentration of the n-type delta doped III-N layer is within a range of 1×10^{13} cm^{-2} to 2×10^{13} cm^{-2}.

6 (Currently amended). The compound semiconductor FET according to Claim 1, wherein material of the substrate is SiC,

wherein each of the semiconductor layers ~~is~~ formed upon the substrate is of a C-plane Ga-surface ~~oriented semiconductor~~ type, and

wherein sheet doping concentration of the n-type delta doped III-N layer is within a range of 5×10^{12} cm^{-2} to 1.5×10^{13} cm^{-2}.

7 (Original). An electronic circuit provided with the compound semiconductor FET as defined in claim 1.